IN THE CLAIMS

1. (Currently Amended) A method of reducing delays in an analog simulation model of a hardware circuit comprising the steps of:

stimulating, via an input, an output of said analog model, wherein said output and said input are coupled by ~~having~~ a relatively high resistance ~~therebetween~~ element; and

applying a pulse to a relatively low resistance element, whereby when said pulse is applied to the relatively low resistance element, the input is connected to said output via the relatively low resistance element so that the time constant of the circuit is reduced.

2. (Currently Amended) A method as claimed in claim 1, wherein the relatively high resistance element is connected in parallel with the relatively low resistance element.

3. (Previously Presented) A method according to claim 1, wherein in said step of applying a pulse, the output is connected to a voltage source having a high drive strength for the duration of the pulse and the voltage source is disconnected before the pulse has time to propagate through the circuit attached to said output.

4. (Currently Amended) A method according to claim 1, further comprising the steps of:

applying a voltage to said input, which is applied to said output via the relatively high resistance element to apply a test voltage having a weak drive strength to the output.

5. (Currently Amended) A method according to claim 4 further comprising the steps of:

providing a delay element operable to provide a delayed control signal and responsive to said delayed control signal disconnecting said relatively low resistance element from between the input and said output.

6. (Previously Presented) A method according to claim 1, in which said analog model is stimulated with an expanded standard logic package.

7. (Original) A method as claimed in claim 6 wherein said method is used when a Z state is present.

8. (Currently Amended) A method according to claim 1, in which said relatively high resistance has a resistance element of between 500 kilo ohms and 1.5 mega ohms.

9. (Currently Amended) A method according to claim 1, wherein said relatively low resistance has a resistance element of between 0.5 ohms and 10 ohms.

10. (Previously Presented) A method according to claim 1, in which said pulse has a duration of between 50 pico seconds to 150 pico seconds.

11. (Previously Presented) A method as claimed in claim 1, wherein said analog model is a SPICE model.

12. (Currently Amended) A system for reducing delays in an analog simulation model of the hardware circuit comprising:

means for ~~stimulation~~ stimulating, via an input, an output of the analog model, said output and said input ~~having~~ being coupled by a relatively high resistance ~~therebetween~~ element; and

means for applying a pulse to a relatively low resistance element, whereby when said pulse is applied to the relatively low resistance element, the input is connected to said output via the relatively low resistance element so that the time constant of the circuit is reduced.

13. (Currently Amended) A computer program comprising code that, when executed on a computer, performs ~~any of the steps of any of claims 1 to 11~~ a method of reducing delays in an analog simulation model of a hardware circuit comprising the steps of:

stimulating, via an input, an output of said analog model, wherein said output and said input are coupled by ~~having~~ a relatively high resistance element; and

applying a pulse to a relatively low resistance element, whereby when said pulse is applied to the relatively low resistance element, the input is connected to said output via the relatively low resistance element so that the time constant of the circuit is reduced.

14. (New) The computer program of claim 13, wherein the relatively high resistance element is connected in parallel with the relatively low resistance element.

15. (New) The computer program of claim 13, wherein in said step of applying a pulse, the output is connected to a voltage source having a high drive strength for the duration of the pulse and the voltage source is disconnected before the pulse has time to propagate through the circuit attached to said output.

16. (New) The computer program of claim 13, wherein the method further comprises the step of:

applying a voltage to said input, which is applied to said output via the relatively high resistance element to apply a test voltage having a weak drive strength to the output.

17. (New) The computer program of claim 16, wherein the method further comprises the step of:

providing a delay element operable to provide a delayed control signal and responsive to said delayed control signal disconnecting said relatively low resistance element from between the input and said output.

18. (New) The computer program of claim 13, in which said analog model is stimulated with an expanded standard logic package.

19. (New) The computer program of claim 18, wherein said method is used when a Z state is present.

20. (New) The computer program of claim 13, in which said relatively high resistance has a resistance element of between 500 kilo ohms and 1.5 mega ohms.

21. (New) The computer program of claim 13, wherein said relatively low resistance has a resistance element of between 0.5 ohms and 10 ohms.

22. (New) The computer program of claim 13, in which said pulse has a duration of between 50 pico seconds to 150 pico seconds.

23. (New) The computer program of claim 13, wherein said analog model is a SPICE model.